Mont-Blanc project: preparing for next-generation supercomputing

Etienne Walter, Mont-Blanc 3 coordinator at Atos shares an expert perspective on how the Mont-Blanc project is preparing for next-generation supercomputing

Arm low-power processors dominate the mobile world of smartphones, tablets and embedded IoT devices. With data centres consuming ever more power, the idea of using highly energy-efficient Arm chips in servers is enticing, especially for energy-hungry high-performance computing (HPC) configurations. As early as 2011, several pioneering European companies and institutions recognised the tremendous potential offered by embedded processor technology and decided to unite into the Mont-Blanc project to investigate the usage of low-power Arm processors for HPC.

Mont-Blanc team receives HPCwire award at SC17

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However, making the leap from the mobile market to HPC was not trivial: HPC-optimised libraries, compilers and applications did not exist for Arm platforms. Mont-Blanc partners had to start from scratch building Arm HPC test systems based on 32-bit mobile phone technology and porting and tuning software and tools to create an Arm software ecosystem. In 2015, Mont-Blanc deployed the world's first Arm-based HPC cluster, featuring over 2,000 mobile CPUs. This system helped demonstrate the viability of using Arm technology for HPC.

Six years on, the landscape has changed dramatically. Arm has introduced its first 64-bit architecture – ArmV8. The Mont-Blanc team put a lot of effort into extending and consolidating the ecosystem developed under the first phase of the project: scientific libraries and runtime systems were ported to ArmV8 and a set of development tools was developed for debugging, performance analysis, performance prediction and automated kernel optimisation.

Interest for Arm processors is rising rapidly in the HPC community, as demonstrated for example by the amount of attention given to all Arm events and announcements at the SC conference in November 2017, or by the HPCwire award received by Mont-Blanc for "Best HPC Collaboration (Academia/Government/Industry)".

Besides purely technological considerations, Arm processors are increasingly viewed as a major asset for Europe's self-determination in HPC, not only by the European Commission, but also by many leading HPC organisations in Europe.

In this favourable context that it contributed to create, the Mont-Blanc project, now in its third phase, is moving ahead. It leverages the findings of the previous project phases to imagine a new high-end HPC platform that will be able to deliver a high-performance/energy ratio whilst executing real applications.

More precisely, the first technical objective of the project is to create a well-bal-

anced architecture and deliver the design for an Arm-based SoC or SoP (System on Package) capable of providing pre-exascale performance – and measured using real HPC applications.

The second objective is to maximise the benefit of this new architecture for HPC applications with new high-performance Arm processors and throughput- oriented compute accelerators designed to work together.

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Finally, the third objective is to develop the necessary software ecosystem for the future SoC – a fundamental asset to maximise the project impact and ensure real life success for this Arm architecture.

For example, one of the issues we are investigating is the need to transform applications from being latency limited to being throughput limited. This was an essential finding of the previous phases of Mont-Blanc. In the same way, kids throw a tantrum to obtain immediately something they desperately need, our programmes issue a request for a resource and stall until whatever they require is available.

Various costly techniques are implemented to achieve some overlap between computation and communication, but our belief is that much more aggressive levels of look-ahead in work/resource demand generation and less urgent synchronisation demands can be achieved by resorting to an asynchronous task-based programming model such as OpenMP4.0 or OmpSs. This transformation from latency-limited (by the response time of individual resource requests) to throughput-limited (by the total amount of resources available) is a key enabler for the future, not only in HPC but also for general purpose computing.

One of the first outcomes of the Mont-Blanc 3 project is a new prototype based on 64-bit ThunderX2 processors from Cavium®, relying on the Arm® v8 instruction set. The system is now live at the Atos R&D centre in Les Clayes near Paris and leverages Atos' Bull Sequana infrastructure, such as cluster management, network, power supply and cooling. It was christened Dibona, after the Dibona peak in the French Alps and the full configuration will ultimately include 48 computes nodes, i.e. 96 Cavium® ThunderX2 CPUs, or 3000 cores.

Dibona is not the end-product of the Mont-Blanc project, but it is a key tool that will allow project partners to expand their research, validate Mont-Blanc performance models and test the completeness and usability of Mont-Blanc's solution. The exciting news about this prototype is that it will not remain a prototype: Atos has decided to productise it and commercialise it as a standard Bull product under the name Bull Sequana X1310.

The Mont-Blanc 3 project is not over yet, but we already know that its outcomes will be put to good use: the Mont-Blanc 2020 project, a spin-off of Mont-Blanc, has just started, with the ambition to pave the way to a European scalable, modular and power efficient high-performance computing.

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Etienne Walter
Mont-Blanc 3 coordinator
Atos
etienne.walter@atos.net
http://montblanc-project.eu/
www.twitter.com/MontBlanc_Eu