MONT-BLANC

Newsletter July 2012

EUROPEAN APPROACH TOWARDS ENERGY EFFICIENT HIGH PERFORMANCE COMPUTING

Mont-Blanc highlighted at ISC2012

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Read full article

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Mont-Blanc collaborates with...

The Partnership for Advanced Computing in Europe (PRACE) is an international non-profit association with its seat in Brussels.

The PRACE Research Infrastructure (RI) provides a persistent world-class High Performance Computing (HPC) service for scientists and researchers from academia and industry. The Implementation Phase of PRACE receives funding from the EU's Seventh Framework Programme (FP7/2007-2013) under grant agreements n° RI-261557 and n° RI-283493.

www.prace-ri.eu

Welcome

Welcome to the first edition of the Mont-Blanc newsletter. As coordinator of the Mont-Blanc project, I first wish to congratulate all the members of the consortium on achieving what is the first step in building a new European Exascale computing approach, based on embedded power-efficient technology. To non Mont-Blanc members, I am thankful for your interest in our research, and the high expectations generated around the project.

Energy efficiency is already a primary concern for the design of any computer system and it is unanimously recognized that future Exascale systems will be strongly constrained by their power consumption. The Mont-Blanc project aims to design a new type of computer architecture capable of setting future High Performance Computing (HPC) standards that will deliver Exascale performance while using 15 to 30 times less energy than today's best designs.

Just as in the past two decades, HPC architectures have been based on commodity server platform technology, in this project we anticipate the ubiquity of today's energy efficient solutions used in embedded and mobile devices as alternate candidates to succeed in the future. The project will define a HPC architecture ex ploiting these and other commodity components together with new programming paradigms capable of supporting future Exascale price, power and performance requirements.

To this end, I hope that this first issue of this Mont-Blanc newsletter is a first step forward to inform about you about the latest news and progresses along this three-year project. Please stay with us as new opportunities for involvement in this research direction will appear in the future.

Alex Ramírez
Mont-Blanc Coordinator

The Mont-Blanc project receives funding from the EU's Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 288777.

Mont-Blanc highlighted at ISC2012

During the International Supercomputing Conference 2012 (ISC'12) held from 17th – 21st of June 2012 in Hamburg (Germany), the Mont-Blanc project was successfully highlighted both at the conference and the exhibition. The ISC Conference is famous for its world-class discussions, with academia and industry leaders tackling the most important HPC issues. Around 300 expert speakers tackles present and future HPC-related issues like Cloud, GPU, Exascale and Energy in tutorials, workshops, keynotes, BoFs, panels and other sessions.

Both Mateo Valero, the BSC Director, and Alex Ramirez, Mont-Blanc project coordinator, were invited to hold a total of two sessions promoting this European project. During all presentations both experts took the opportunity to give further details about the latest results in Mont-Blanc, that has become one of the hot topics among the HPC community.

On Tuesday 19th June, Prof. Mateo Valero, was invited to an 1 ½ hour invited session under the title "Mont-Blanc, European Approach towards Energy Efficient HPC". He took the opportunity to raise the widely recognized power-issue of the Exascale systems. In his talk, he reviewed the design philosophies of several vendors, including HPC compute accelerators, and ARM-based mobile application processors in terms of peak performance, memory bandwidth, and energy efficiency; and he reviewed how the OmpSs programming models exploits the benefits of the Mont-Blanc approach while overcoming the drawbacks.

The second conference disseminating the project was on Wednesday 20th with a satellite event under the title "The European Way to Exascale – Presentation of the EU Funded Exascale Projects". Alex Ramirez highlighted the Mont-Blanc system architecture to achieve the expected energy-efficiency objective: how chips and memory will be packaged, and connected together in a competitive performance system architecture, with leading energy efficiency. As previously announced the system will be based on the ARM processor architecture, but it has not yet selected the final silicon to power the system. In this presentation he also took the opportunity to give an overview on the selection criteria for the energy-efficient ARM-based chip to be integrated in the Mont-Blanc prototype.

Finally, the Mont-Blanc project was also promoted at the ISC'12 exhibition hall at the booths of Bull, Gnodal, Leibniz Supercomputing Center, and Barcelona Supercomputing Center with Mont-Blanc posters and flyers.

The Barcelona Supercomputing Center booth at ISC2012 in Hamburg, Germany

Mont-Blanc selected one of the most innovative projects by Ecotendències CosmoCaixa

The European Project Mont-Blanc has been selected as one of the most innovative projects under the section "Moure Informació" (Moving Information) of the Ecotendències Cosmocaixa Awards. The award recognizes the impact of innovative ideas, as well as their environmental impact in the Spanish region of Catalonia.

The jury was composed by the l'Àrea de Ciència, Recerca i Medi Ambient i l'Àrea d'Emprenedoria de "la Caixa" (Area of Science, Research and Environment of the Catalan Bank "La Caixa", The Barcelona City Council, Barcelona Digital Technological Centre and the Studio Ramon Folch and Associates S.L.). The challenge of the Mont-Blanc project is to deploy an energy efficient HPC system based on technology used in mobile devices or tablets.

During the presentation at the premises of the Science Museum in Barcelona CosmoCaixa, Alex Ramirez, coordinator of the Mont-Blanc project and team leader of The Heterogeneous Architectures Group at the Barcelona Supercomputing Center – Centro Nacional de Supercomputación (BSC-CNS), gave a brief overview of the project's aims. "Computer performance is already limited by energy consumption. In this project, we aim to exploit technologies originally developed for the mobile market to develop a new class of energy-efficient supercomputers. This award recognizes the daily work of a European consortium and a multidisciplinary team, that could change the way we understand supercomputers today, in a similar way to what happened with microprocessors at the end of the 90s", says Ramírez.

The event finished with a debate between all attendees and the participants of the 11 selected projects about the use of new technologies and its environmental impact reduction. This debate was moderated by Miquel Huguet, Director of the Center for Scientific and Academic Services of Catalonia (CESCA).

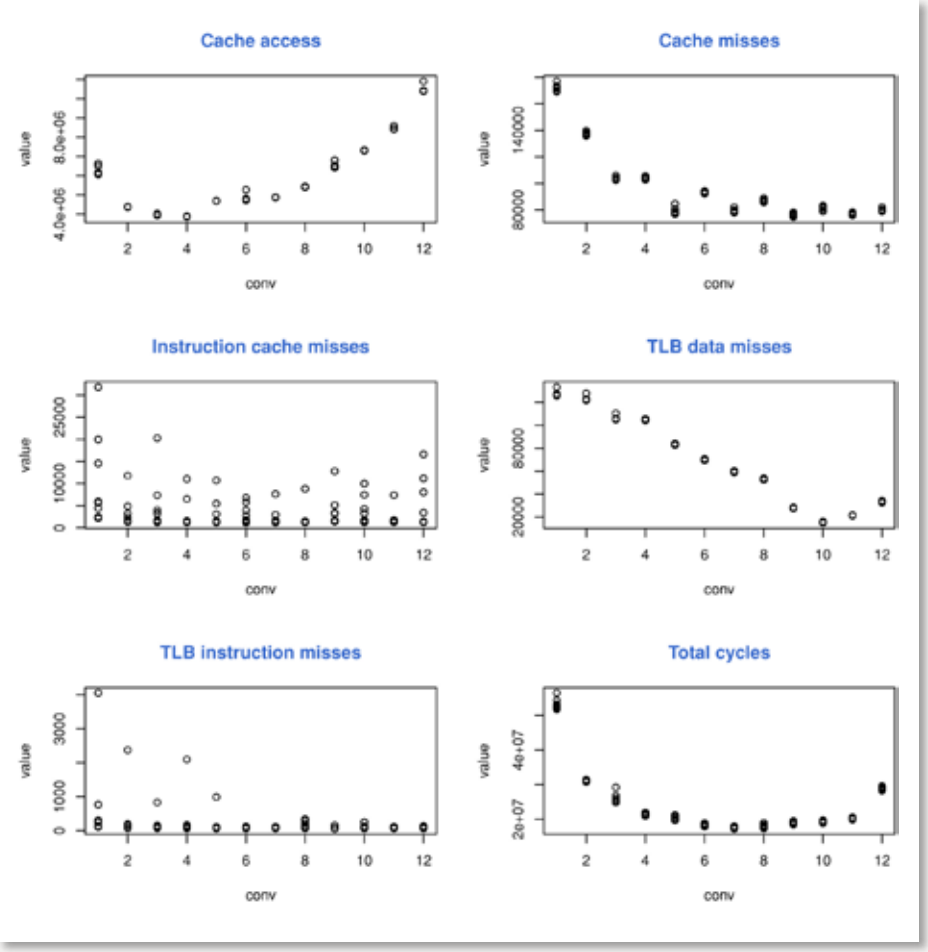
Pictures of the event:

https://www.facebook.com/media/set/?set=a.315834815157792.71399.220070118067596&type=1

Alex Ramírez at the Science Museum in Barcelona CosmoCaixa

Application kernels to drive ARM innovation in High Performance Computing

The Mont-Blanc project aims at achieving stunning breakthroughs towards the energy-efficiency of HPC systems by combining the ARM architecture with a task based programming model (OmpSs) capable of providing an abstract framework for the programmer to work with. To ensure an effective exploration of these new technologies, a set of kernels (i.e. portions of a program that are well-defined from the algorithmic standpoint and present a clear pattern of computation and/or communication) has been recently selected and will be used as a test-bed in the forthcoming work.



Influence of the loop unrolling factor on BigDFT magic filter, when the outer loop is unrolled with steps varying from 1 to 12.

The selection process was the result of an in-depth profiling involving most of the 11 applications that are part of MontBlanc, and has been guided mainly by the attempt to maximize the impact that the to-be-learned best-practices will have on real production applications. The final outcome is a set of three small-size kernels (FFT, complex Hermitian matrices diagonalization, solution of sparse linear system) and five medium-size kernels which cover a wide spectrum of scientific areas (material science, molecular dynamics, weather prediction, etc.). During the selection phase a particular care has been taken to correctly identify the codes that could benefit from taskification of their execution (such as COSMO, a widely used weather prediction application) and the algorithms that may be optimized using techniques that are peculiar to the ARM architecture. In this sense a remarkable achievement has been the tuning of the magicfilter algorithm of BigDFT (an ab-initio simulation software) using a loop unrolling technique that permits the best exploitation of the floating point units of the ARM processor. The figure above shows that the impact on performance is quite important, providing an improvement by a factor 2.5 compared to the non-unrolled version. In the incoming months all of the selected kernels will be ported to the OmpSs programming model and then optimized at a low architectural level in their performance-critical parts. Hopefully the knowledge gained operating on these representative, yet simple, pieces of codes will be transferred to full-scale applications by the end of the project.